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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,800	11/08/2001	Mark A. Gerber	SC11588TK	7112

23125 7590 06/02/2004

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EXAMINER	
ROMAN, ANGEL	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,800	GERBER ET AL.	
	Examiner	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 28-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7,11-15,28,30-40 and 43-50* is/are rejected.

7)☒ Claim(s) *3-5,8-10,29,41 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: In line 6, "the first plane" should be replaced with --the second plane-- since the tape is attached along the second plane; in line 13 "the first pads" should be replaced with --first pads-- and in line 15 "the second pads" should be replaced with --second pads--, since there is no antecedent basis for these claim limitations. Appropriate correction is required.

2. Claim 3 is objected to because of the following informalities: In line 13, "the encapsulating" should be replaced with --encapsulating--. Appropriate correction is required.

3. Claims 4 and 5 are objected to for their dependency on claim 3.

4. Claim 43 is objected to because of the following informalities: In line 8 "test pads" should be replaced with --pads--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 6, 11, 12, 30, 31, 35-37 and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Eng et al. U.S. Patent 5,798,564 A.

Eng et al. discloses a method for forming a package device comprising; providing a package substrate 12 having a first surface along a first plane and a second surface along a second plane (see figure 1), wherein the package substrate 12 has a cavity 12b between the first plane and the second plane and is not form from encapsulating material; placing a first integrated circuit 16 in the cavity 12b (see figure 2); placing a second integrated circuit 25 adjacent to the first integrated circuit 16 outside the cavity 12b, such that die attach material 24 (see column 2, lines 10-12) is interposed between the first integrated circuit 16 and the second integrated circuit 25; and depositing encapsulating material (27a, 28b) over the first integrated circuit 16 and the second integrated circuit 25, the encapsulating material not overlying at least one pad. The package substrate further comprises a supporting member 13 along the second plane of the substrate and between the first integrated circuit 16 and the second integrated circuit 25 (see figure 3). Eng et al. also discloses electrically connecting the first integrated circuit 16 to first pads 19 located on the first surface; electrically

connecting the second integrated circuit 25 to second pads located on the second surface, wherein the electrically connecting comprises wire bonding (see figure 3); and depositing a first portion of encapsulating material over the first integrated circuit prior to the step of placing the second integrated circuit, and depositing a second portion of the encapsulating material over the second integrated circuit (see figures 1-3).

7. Claims 6, 11-13, 30-32 and 35-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. U.S. Patent 6,344,687 B1.

Huang et al. discloses a method for forming a package device, comprising; providing a package substrate 200 having a first surface along a first plane and a second surface along a second plane (see figure 4), wherein the package substrate has a cavity between the first plane and the second plane (see figure 6); placing a first integrated circuit 240 in the cavity; placing a second integrated circuit 220 adjacent to the first integrated circuit 240 outside the cavity, such that a conductive supporting member 232 is interposed between the first integrated circuit 240 and the second integrated circuit 220; and depositing encapsulating material (230, 250) over the first integrated circuit 240 and the second integrated circuit 220, wherein the package substrate 200 is not formed from encapsulating material (see figure 7). Huang et al. also discloses die attach material interposed between the first integrated circuit 240 and the second integrated circuit 220 (see column 3, lines 50-56) and electrically connecting the

first and second integrated circuits to pads (204, 206, 210) on the first and second surfaces, wherein the connection is by wire bonding.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 1, 2, 30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. U.S. Patent 6,515,356 B1 in view of Higgins III U.S. Patent 5,291,062 A.

Shin discloses a method for forming a package device, comprising; providing a package substrate 10 having a first surface along a first plane, wherein the package substrate 10 has a cavity between the first plane and the second plane; attaching a tape 40 (supporting member) to the package substrate 10 along the second plane; placing a first integrated circuit 2 on the tape and in the cavity (see figure 2); depositing encapsulating material 20 over the first integrated circuit; removing the tape; placing a second integrated circuit 3adjacent to the first integrated circuit outside the cavity (see figure 6A); depositing encapsulating material over the second integrated circuit 3; electrically connecting the first integrated circuit to first pads 15, wherein the first pads are located on the first surface; and electrically connecting the second integrated circuit to second pads, wherein the second pads are located on the second surface, wherein the encapsulating material does not overlie any of the pads. Shin et al. also discloses depositing the encapsulating materials using a transfer

molding process (see figure 13) and an optional conductive supporting member. Shin is applied as above but lacks anticipation on disclosing at least one of the pads accessible for testing purposes. Shin et al. discloses forming solder balls 30 on the pads 15, therefore the pads 15 would be available for testing before forming the solder balls 30, therefore, it would have been obvious to one having ordinary skills in the art at the time the invention was made to disclose the pads accessible for testing in the primary reference of Shin et al.. Furthermore Higgins III discloses testing an integrated circuit before completing a packaging process; it would have been obvious to a person having ordinary skills in the art at the time the invention was made to test the integrated circuit disclose in Shin et al. using the testing method disclose in Higgins III thereby having the pads disclosed in Shin et al. available for testing purposes, in order to reduce process costs related to unnecessary packaging of non-functional integrated circuits, e.g. forming solder balls on the pads.

12. Claims 6, 7, 11, 14, 15 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. U.S. Patent 6,515,356 B1 in view of Lin et al. U.S. Patent 5,273,938 A.

Shin et al. disclose all the subject matter described above in paragraph 9 but lacks anticipation on disclosing die attach material interposed between the first integrated circuit and the second integrated circuit. Lin et al. discloses a method of forming a package integrated circuit by bonding a second integrated circuit 21 to a first integrated circuit 21 using a die attach material 22 (see figure

4). In view of this disclosure it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use a die attach material interposed between the first integrated circuit and the second integrated circuit in the primary reference of Shin et al. in order to insulate the integrated circuits from each other and to provide mechanical stability during a subsequent encapsulating process and thereby prevent damage to the second integrated circuit (see Lin et al., column 4, lines 49-56).

13. Claims 43-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi U.S. Patent 6,291,892 B1 in view of Higgins, III U.S. Patent 5,291,062 A.

Yamaguchi discloses a method of forming a package device, comprising; providing a package substrate 12 having a first side and a second side; providing first pads (11a) on the first side and second pads (11a) on the second side, the substrate having a cavity (see figure 22); and providing a first integrated circuit (10) mounted to the package substrate 12 inside the cavity and connected to the first pads, and wherein one of the first and second pads is not covered by an encapsulating material 15 and is exposed (see figure 22). Yamaguchi et al. also discloses providing a second integrated circuit 10 mounted to the package substrate 12 adjacent to the second first integrated circuit 10 and connected to the second pads, wherein the second integrated circuit is mounted to the substrate by adhesive die attached tape 8 and a second die attached material

supporting member 8 is between the first integrated circuit 10 and the second integrated circuit 10 (see figure 22).

Yamaguchi is applied as above but lacks anticipation on indicating that the first pads and the second pads are further characterized as being useful for receiving test probes for testing. Higgins III, discloses a method for making and testing a package device having pads 18 characterized as being useful for receiving test probes for testing (see column 5, lines 32-37). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to test the integrated circuit in the primary reference of Yamaguchi by applying test probes to the pads 11a and thereby characterizing the pads useful for testing as disclose in Higgins, III in order to determine integrated circuit functionality and to further reduce process costs by preventing unnecessary packaging of non-functional integrated circuits.

14. Claims 38 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eng et al. U.S. Patent 5,798,564 A in view of Higgins, III U.S. Patent 5,291,062 A.

Eng et al. is applied as above but lacks anticipation on testing the first and second integrated circuit by applying test probes to the first and second pads; and disclosing a transfer molding process for depositing the encapsulating material.

With respect to testing the first and second integrated circuit by applying test probes to the first and second pads Higgins, III discloses testing an

integrated circuit by applying test probes to pads, therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to test the integrated circuits disclosed in Eng et al. by using the method of Higgins, III since it would reduce manufacturing costs.

Regarding using a transfer molding process to deposit the encapsulating material in the primary reference of Eng et al., it would have been obvious to a person having ordinary skills in the art at the time the invention was made to deposit the encapsulating material in the process disclosed by Eng et al. using a transfer molding process in order to mold the encapsulating material on desire package locations.

Allowable Subject Matter

15. Claims 3-5 would be allowable if rewritten or amended to overcome the objection set forth in this Office action.

16. Claims 8-10, 29, 41 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

17. Applicant's arguments with respect to amended claim 1, the rejections of claims 2-5, 8-10 28 and 29 under 35 U.S.C. 103(a), and claims 30 and 31 have been considered but are moot in view of the new ground(s) of rejection.

18. Applicant's arguments filed 02/24/04 have been fully considered but they are not persuasive. Regarding Applicant's argument that reference number 22 in Lin et al. are wire bonds, this argument is incorrect since Lin et al. clearly teaches using die attach material 22 (see Lin et al. figures 4-7).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cho, Gallas and Terui disclose method for forming package devices having integrated circuits on opposite sides of a substrate, wherein on of the integrated is in a substrate cavity.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (571) 272-1681. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
May 26, 2004

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